



# 5th IEEE International Workshop on Silicon Debug and Diagnosis 2008

## *Final Program*

Day 1 : April 30 <sup>th</sup> 2007		
4:00 PM	4:15 PM	<b>Opening remarks</b>
<ul style="list-style-type: none"> <li>• <b>Fidel Muradali</b> (National Semiconductor)</li> <li>• <b>Bart Vermeulen</b> (NXP Semiconductors)</li> </ul>		
4:15 PM	5:30 PM	<b>Paper Session 1</b> Chair: Ismed Hartanto (Xilinx)
<ul style="list-style-type: none"> <li>• “Silicon debug of timing failures with debug-oriented scan test patterns”, Christian Burmer<sup>1</sup>, <b>Ruifeng Guo</b><sup>2</sup>, Wu-Tung Cheng<sup>2</sup>, Xijiang Lin<sup>2</sup>, Brady Benware<sup>2</sup> (<sup>1</sup>Infineon, <sup>2</sup>Mentor Graphics)</li> <li>• “Targeting Leakage Constraints during ATPG”, Görschwin Fey<sup>1,2</sup>, <b>Satoshi Komatsu</b><sup>1</sup>, Yasuo Furukawa<sup>3</sup>, Masahiro Fujita<sup>1</sup> (<sup>1</sup>University of Tokyo, <sup>2</sup>University of Bremen, <sup>3</sup>Advantest)</li> <li>• “An Industrial Case Study of Diagnosing Randomly Distributed Chain Defects for Process and Yield Improvement”, Gunaseelan Ponnuvel<sup>1</sup>, Mark Grosset<sup>1</sup>, <b>Yu Huang</b><sup>2</sup>, Wu Yang<sup>2</sup> (<sup>1</sup>Conexant System, <sup>2</sup>Mentor Graphics)</li> </ul>		
5:30 PM	5:45 PM	<b>Break</b>
5:45 PM	5:50 PM	<b>Soapbox - Haluk Konuk</b> (Broadcom)
5:50 PM	6:40 PM	<b>Special Session 1</b> Chair: Teresa McLaurin (ARM)
<ul style="list-style-type: none"> <li>• “IEEE P1687 Update – Inside the Chip”, <b>Al Crouch</b> (Asset Intertech)</li> <li>• “Post silicon debug and validation of a multi-million gate high-definition digital TV controller”, <b>Miron Abramovici</b> (DAFCA)</li> </ul>		
7:00 PM	9:00 PM	<b>Social Event</b>

Day 2 : May 1 <sup>st</sup> 2007		
8:00 AM	8:45 AM	<b>Keynote</b> Chair: Bart Vermeulen (NXP Semiconductors)
<ul style="list-style-type: none"> <li>• <b>Nitin Deo</b> (Cadence Design Systems)</li> </ul>		
8:45 AM	10:00 AM	<b>Paper Session 2</b> Chair: Mike Ricchetti (AMD)
<ul style="list-style-type: none"> <li>• “An Automated Software Solution to Silicon Debug”, Yu-Shen Yang<sup>1</sup>, Andreas Veneris<sup>1</sup>, <b>Nicola Nicolici</b><sup>2</sup> (<sup>1</sup>University of Toronto, <sup>2</sup>McMaster University)</li> <li>• “Methodology for Hardware/Software co-debug”, <b>Gertjan Arnoldussen</b><sup>1</sup>, Hans Kok<sup>2</sup> (<sup>1</sup>Philips, <sup>2</sup>NXP Semiconductors)</li> <li>• “A New Approach for Capturing Trace Data from SoCs”, <b>Alexander Weiss</b><sup>1</sup>, Christian Hochberger<sup>2</sup> (<sup>1</sup>Accemic GmbH, <sup>2</sup>Univ. of Technology Dresden)</li> </ul>		
10:00 AM	10:30 AM	<b>Break</b>





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10:30 AM	12:00 PM	<b>Paper Session 3</b> Chair: Davide Appello – STMicroelectronics
<ul style="list-style-type: none"> <li>• “<i>Rapid Navigation for Semiconductor Failure Analysis Without Requiring Layout vs. Schematic (LVS) Information</i>”, <b>Roger Nicholson</b>, Hitesh Suri (DCG Systems)</li> <li>• “<i>A Learning of Process Interacted Silicon Debug of UltraSPARC T2 Microprocessor</i>”, <b>Poh-Joo Tan</b> (Sun Microsystems)</li> <li>• “<i>Hardware/Software Co-Design/Execution Approach to Silicon Debug and Diagnosis</i>”, <b>Masahiro Fujita</b>, Hiroaki Yoshida Satoshi Morishita (University of Tokyo) (S)</li> <li>• “<i>An Efficient and Cost Effective Methodology for Post Silicon Test Pattern Generation</i>”, <b>Andy Chang Seow Pin</b>, Lee Khim-Hou (Infineon) (S)</li> </ul>		
12:00 PM	1:30 PM	<b>Lunch</b>
1:30 PM	2:20 PM	<b>Special Session 2</b> Chair: Nicola Nicolici (McMaster Univ.)
<ul style="list-style-type: none"> <li>• “<i>The role that ATE can play in Silicon Debug and Diagnosis</i>”, <b>Don Blair</b> (Verigy)</li> <li>• “<i>Boosting yield learning by leveraging advanced design automation during failure analysis</i>”, <b>Simona Pappalardo</b> (ST Microelectronics)</li> </ul>		
2:20 PM	3:35 PM	<b>Paper Session 4</b> Kazumi Hatayama (STARC)
<ul style="list-style-type: none"> <li>• “<i>A case study on SoC low-cost Silicon Debug and Diagnosis</i>”, D. Appello<sup>1</sup>, M. Rotigni<sup>1</sup>, V. Tancorre<sup>1</sup>, P. Bernadi<sup>2</sup>, <b>M. Grosso</b><sup>2</sup>, M. Sonza Reorda<sup>2</sup>, (<sup>1</sup>ST Microelectronics, <sup>2</sup>Politecnico Torino)</li> <li>• “<i>Study on Hardware Overhead Reduction for Memory BIST</i>”, Kentaro Osawa<sup>1</sup>, Masayuki Arai<sup>1</sup>, <b>Kazuhiko Iwasaki</b><sup>1</sup>, Michinobu Nakao<sup>2</sup>, (<sup>1</sup>Tokyo Metropolitan University, <sup>2</sup>Renesas Technology)</li> <li>• “<i>A Novel Hardware Description language for efficient debug and diagnosis of digital circuits</i>”, <b>Michele Portolan</b><sup>1</sup>, Suresh Goyal<sup>1</sup>, Brad Van Treuren<sup>2</sup>, Chen-Huan Chiang<sup>2</sup>, Tapan Chakraborty<sup>2</sup> and Tom Cook<sup>2</sup> (<sup>1</sup>Bell Labs Ireland, <sup>2</sup>Alcatel-Lucent Bell Labs)</li> </ul>		
3:35 PM	3:50 PM	<b>Break</b>
3:50 PM	3:55 PM	<b>Soapbox - Doug Josephson</b> (Intel)
3:55 PM	4:45 PM	<b>Special Session 3</b> Chair: Teresa McLaurin (ARM)
<ul style="list-style-type: none"> <li>• “<i>Innovation from Debug: Creatively Reducing a Ground Loop</i>”, <b>Hugh Weinrich</b> (National Semiconductor)</li> <li>• “<i>Debug and Diagnostic Data for Yield Learning</i>”, <b>Jay Orbon</b> (Verigy)</li> </ul>		
4:45 PM	5:00 PM	<b>Wrap-up</b>
<ul style="list-style-type: none"> <li>• <b>Fidel Muradali</b> (National Semiconductor)</li> <li>• <b>Bart Vermeulen</b> (NXP Semiconductors)</li> </ul>		

(S) = Short paper, **bold** = Designated Speaker

