6th IEEE International Workshop on Silicon Debug and Diagnosis

FINAL PROGRAM

■ 08:30 - 09:15 Session 1: Opening

Welcome Address and Opening Remarks
Bart Vermeulen, NXP Semiconductors – General Chair
Al Crouch, ASSET Intertech – Program Co-Chair
Christian Boit, TU Berlin – Program Co-Chair

Keynote Address:
Debug and Diagnosis Challenges for New Technology Yield Ramp
Thomas Hermann, Global Foundries, Germany

■ 09:15 - 10:15 Session 2: Post Silicon Validation

09:15 - 09:35 - Building a Bridge: From Pre-Silicon Verification to Post-Silicon Validation, Amir Nahir, Allon Adir, Charles Meissner, Gil Shurek - IBM Research Haifa University, Haifa, IL
09:35 - 09:55 - Post-Silicon Debug of Complex Multi Clock and Power Domain SoCs, Bradley R Quinton, Andrew M Hughes, Steven J E Wilton - University of British Columbia, US
09:55 - 10:15 - Guaranteeing Coverage in Post-silicon Validation, Amir Nahir, Allon Adir, Avi Ziv, Charles Meissner, John Schumann - IBM Research, Haifa University, Haifa, IL

■ 10:15 - 10:30 Embedded Tutorial 1

10:15 - 10:30 - JTAG-Based Data Collection, John Potter, ASSET, Texas, US

■ 10:30 - 11:00 Coffee and tea break

■ 11:00 - 12:00 Session 3: Test and Debug Algorithms

11:00 - 11:20 - Automated Silicon Debug Analysis Techniques for a Hardware Data Acquisition Environment, Yu-Shen Yang, Brian Kang, Andreas Veneris, Nicola Nicolici, Hratch Mangassarian - University of Toronto, Toronto, CA

11:20 - 11:40 - Efficient Methods for Debug of ATPG Scan Chain Failures on ATE, Ernst Aderholz -- Freescale Semiconductor, Munich, DE

11:40 - 12:00 - A Cumulative Memory Failure Bitmap Display & Analysis SW Tool
P Bernardi, A Panariti, M Sonza Reorda, T Kerekes, D Appello, M Barone - Politecnico di Torino, IT

■ 12:00 Lunch break

■ 13:00 - 13:30 Embedded Tutorials 2 + 3

13:00 - 13:15 - Part 1: Debug Methodology: Does One Size Fit All, Geir Eide, Mentor Graphics

13:15 - 13:30 - Part 2: Debug Methodology: Advances in ASIC Fault Isolation, Antonino Barna, Andrea Bogliolo; Carlo Caimi; Alberto Pintus - STMicroelectronics, IT

■ 13:30 - 14:30 Session 4: Physical Root-cause

13:30 - 13:50 - Physical Fault Isolation on Large Designs using a Hybrid Logical-to-Physical Cross Mapping Solution, Cathy Kardach, Hitesh Suri, DCG Systems Inc, Fremont, CA, US, Puneet Gupta, Tung Ton, NVIDIA Corp., Santa Clara, CA, US

13:50 - 14:10 - Fault Localization on Scan Designs using Analog Simulation, Christian Burmer, Andreas Altes, Markus Gruetzner, Thomas Schweinboeck, Infineon Technologies, Munich, DE

14:10 - 14:30 - Local IC Speed Trimming, Nanoscale CE and Analysis Based upon a Coaxial Optical and Ion Beam Approach, Christian Boit, R Schlangen, U Kerst, T Lundquist, University of Berlin, DE

■ 14:30 - 15:00 Coffee and tea break

■ 15:00 - 16:30 Panel Session: Formalized Debug-Diagnosis versus Ad Hoc Methods

Description: The panel will wrestle with the question of "has the debug-diagnosis problem reached, or is it about to reach, a level of complexity that requires a formal industry-wide standard solution - or can it continue with each chip from each chip provider having none, some, or a different mix of DFT and DFD solutions?" If a standard solution is needed, what are the requirements and who drives those requirements? If each chip provider or core provider can support its own DFT and DFD solutions, how do these solve the "mixed-resource" problem that exists in complex SoCs and 3D chips? How can end users with No Trouble Found (NTF) and Cannot-Repeat (CNR) replicate problems if the resources are not easily operated concurrently? The panel members will each take a stance and will justify that stance against the issues and requirements of their own industry sector.

Moderator: Al Crouch – ASSET Intertech, Texas, US

Panelists: Invited Panelists consisting of representatives from EDA, SoC, ATE, Microprocessor, and 3D Stacked-die.

■ 16:30 Conclusion and close

Al Crouch, ASSET Intertech – Program Co-Chair
Christian Boit, TU Berlin – Program Co-Chair
Bart Vermeulen, NXP Semiconductors – General Chair