

DATE 2010 Friday Workshop

6th IEEE International Workshop on Silicon Debug and Diagnosis



March 12th, 2010 - Dresden, Germany

General Chair

B. Vermeulen - NXP Semiconductors

Program Co-chairs

C. Boit - TU Berlin

A. Crouch - ASSET Intertech

Asian Liaison

K. Hatayama - STARC

European Liaison

D. Appello - STMicroelectronics

North-American Liaison

T. McLaurin - ARM

University Liaison

Z. Zilic – McGill Univ.

Electronic Media

I. Bayraktaroglu - Sun

Local Arrangements

P. Cheung - Imperial College London

N. Nicolici - McMaster Univ.

Program Committee

M. Abadir – Freescale

M. Abramovici - DAFCA

- B. Benware Mentor Graphics
- V. Bertacci Univ. of Michigan
- S. Blanton Carnegie Mellon Univ.
- B. Cory nVidia
- B. Eklow Cisco Systems
- J. Giacobbe Intel
- R. Guo Mentor Graphics
- S. Gupta USC
- I. Hartanto Xilinx
- Y-C. Hsu SpringSoft
- D. Josephson Intel
- R. Kapur Synopsys
- H. Kerkhoff Univ. Twente
- C. Metra Univ. Bologna
- A. Orailoglu UCSD
- S. Pappalardo STMicroelectronics
- P. Prinetto Poli. Di Torino
- M. Renovell LIRMM
- M.S. Reorda Poli. Di Torino
- N. Stollon HDLdynamics
- C. Sul Silicon Image
- J. Tyzer U. Poznan
- S. Venkataraman Intel
- Z. Zilic McGill Univ.

Steering Committee

- R. Aitken ARM
- E.J. Marinissen IMEC
- F. Muradali National Semiconductor
- M. Ricchetti AMD (chair)
- Y. Zorian Virage Logic

Call for Papers

Scope and Mission

Troubleshooting how and why systems and circuits fail is important and is rapidly growing in industry significance. Debug and diagnosis may be needed for yield improvement, process monitoring, correcting the design function, failure mode learning for R&D, or just getting a working first prototype. This detective work is however very tricky. Sources of difficulty include circuit and system complexity, packaging, limited physical access, shortened product creation cycle and time-to-market, the traditional focus on only pass/fail testing and missing tool and equipment capabilities. New and efficient solutions for debug and diagnosis have a much needed and highly visible impact on productivity.

The topics of interest include, but are not limited to, the following:

- Debug Techniques and Methodologies
- Design and Synthesis for Debug
- DFT Reuse for Debug and Diagnosis
- Debug & Diagnosis Architectures
- Tools
- Debug Standardization
- SDD vs. Yield & TTM
- Case studies

- Microprocessor, FPGA, IP, SOC Debug
- Infrastructure IP for SDD
- System Level Debug & Diagnosis
- Manufacturing & Prototype Environment
- Equipment Impact and Techniques
- Cross-geography turn-on, debug & diagnosis issues
- Digital / Analog Turn-on

Author Information

The workshop objective is to facilitate a valuable interactive information exchange. Contributions ranging from extended abstracts to full papers are acceptable for submission. Proposals that describe open issues, industry/technology needs or opinions are also welcome.

- Length Guideline: ranging from a one page, extended abstract up to 8 pages.
- Submissions due: November 6th, 2009
- Acceptance Notification: November 20th, 2009
- Final papers for inclusion into informal proceedings: March 3rd, 2010

Proposals for discussion panels and other special sessions are also invited. Please submit a one page abstract for these to the web site or contact the Program Co-chairs.

General information: Submission & program information:

Bart Vermeulen Christian Boit Al Cro

NXP Semiconductors Berlin University of Technology ASSET Intertech

<u>bart.vermeulen@nxp.com</u> <u>christian.boit@tu-berlin.de</u> <u>acrouch@asset-intertech.com</u>

SDD'10 is sponsored by the IEEE Computer Society Test Technology Technical Council. For more information on SDD'10, visit the website at: http://www.sdd-online.org





