7th IEEE International Workshop on Silicon Debug & Diagnosis – SDD2011
September 22nd – 23rd, Anaheim, California

Day 1 – September 22nd

4:00 – 4:15pm – Opening Remarks – *T. McLaurin, ARM, I. Hartanto, Xilinx*

4:15pm – 4:45 pm – Keynote Address
"Can 3D Extend Moore's Law Better than Process Shrinks or will Test, Debug-Diagnosis, and Security Prevent it?" – Al Crouch, ASSET InterTech, Inc.

4:45pm – 5:15 pm – Invited Address
"Is Physical Debug Running out of Photons, Electrons, and Ions? The Challenges at the 22nm Technology Node and Below" – John Giacobbe, Intel

5:15pm – 6:00pm:
Experience & Opinion – Fidel Muradali, National Semiconductor

Session 1:
6:00pm – 6:30pm

Paper 1.1 – Efficient Post-Silicon Verification and Debugging with Patchable/Programmable Accelerators Synthesized from High Level Designs – *M. Fujita, Univ. of Tokyo*

Workshop Welcome Reception - 7:00pm – 9:00pm

Day 2 – September 23rd

Session 2:
8:30am – 10:00am

Paper 2.1 – Understanding ATE capabilities to leverage during silicon debug. – *N. Dakwala, Broadcom*
Paper 2.2 – Extending Constrained Random Verification to mixed-signal Automotive Power Devices using a non-stationary Markov Process – *T. Nirmaier, M. Harrant, G. Pelz, Infineon AG*
Paper 2.3 – New Approaches for Analysis of Logic Fail Data – *V. Tancorre, D. Appello, R. Dokken, ST Micro & Roguevation*

Session 3: Chair – E. Rentschler, AMD
10:30am –12:00noon

Panel Discussion: "Digital test is a solved problem! The future must focus on post-silicon validation and debug"
Davide Appello – ST Micro
CJ Clark – Intellitech
Bob Gottlieb – Intel
Greg Lewis – AMD
Neal Stollon – HDL Dynamics

Lunch - 12:00 pm – 1:30pm

Session 4:
1:30pm – 3:30pm

Paper 4.1 – Failing within Passing Region – *S. Kumar, Broadcom*

Paper 4.2 – Exploring CΔIDDQ Bridging Defect Diagnosis Capabilities – *C. Thibeault, Y. Hariri, H. Khaled, Ecole de Technologie superieure*

Paper 4.3 – Yield, Reliability, Lasers, and Shift Defect Isolation, *S. Kasapi, J. Liao, NVIDIA*

Paper 4.4 – Evolution of CAD for Silicon Debug: from the IDM FA Lab to the Fabless and Foundry Yield Collaboration, *C. Kardach, H. Suri, J. Gade, DCG Systems*

3:30pm – 3:45pm:

Experience & Opinion – Fidel Muradali, National Semiconductor

3:45 – 4:00pm – Closing Remarks – *T. McLaurin, ARM, I. Hartanto, Xilinx*