# 8th IEEE International Workshop on Silicon Debug and Diagnosis – SDD 2012

**Thursday November 8th – Friday November 9th**
**Anaheim, California**

**Immediately following the 2012 International Test Conference**

## Invited Talks

**Thursday, November 8th**

16:15 Keynote Talk
"*Post-Silicon Debug and Validation in the Billion Transistor SoC Era*"
**Eric Rentschler**, Fellow at AMD

Abstract:
Pre-silicon design and verification techniques and process technology have enabled today's multi-billion FET designs. Market forces have driven features, form factor, price, power and performance, leading to designs with a functional state-space of astronomical proportions. Post silicon debug and validation techniques have not kept pace, leading to high risk of late bug discovery and longer time-to-market that is not adequately addressed today. In this talk, we will explore current challenges and define a vision for how the industry can address the increasing challenges faced by today's SoC teams.

Speaker's Bio: Eric Rentschler is a Fellow at AMD, where he has led the Design-for-Debug/Validation group since 2006. He has over 24 years of experience in the industry, also including Intel and HP. He has worked on 3D graphics accelerators, memory controllers, chipsets and CPUs. Over the past decade he has focused more on system-level debug and validation. He holds 24 US patents in areas including caching algorithms, RAS features, memory controllers and debug features. He holds degrees from Bowling Green State University and the University of Michigan.

**Friday, November 9th**

08:00 Invited Address
"*Improving Design, Manufacturing and Even Test through Test-Data Mining*"
**Shawn Blanton**, Professor of ECE and Director of the Center for Silicon System Implementation at Carnegie Mellon University

Abstract:
For many years now, the Advanced Chip Test Laboratory (www.ece.cmu.edu/~actl) at Carnegie Mellon has been using layout information for improving manufacturing test, in particular, for changing test from a sort-only task to one that also involves learning about the design, the manufacturing process, and their interaction through testing to produce high-yielding, high-quality chips. The underlying technology for our work has been what we call physically-aware diagnosis. In this approach to diagnosis, the goal is not only localization but a physical characterization of the defect and its corresponding faulty behavior. This is accomplished by a data-driven extraction of a failure model that is based on a systematic analysis of the layout and the test data. In this talk, physically-aware diagnosis will be contrasted with conventional approaches to demonstrate the improvement in resolution and accuracy that can be gained through limited layout analysis. Some of the benefits of physically-aware diagnosis will then be demonstrated using METER (MEasuring Test Effectiveness Regionally), a technique for evaluating fault models and test metrics using readily-available tester data from production ICs.

Speaker's Bio: Shawn Blanton is a professor in the Department of Electrical and Computer Engineering at Carnegie Mellon University where he serves as director of the Center for Silicon System Implementation (CSSI), an organization consisting of 18 faculty members and over 80 students focused on the design and manufacture of silicon-based systems. He received the Bachelor's degree in engineering from Calvin College in 1987, a Master's degree in Electrical Engineering in 1989 from the University of Arizona, and a Ph.D. degree in Computer Science and Engineering from the University of Michigan, Ann Arbor in 1995.

Professor Blanton's research interests include the verification, test and diagnosis of integrated, heterogeneous systems. He has published over 100 papers in these areas and has several issued and pending patents in the area of IC test and diagnosis. Prof. Blanton has received the National Science Foundation Career Award for the development of a microelectromechanical systems (MEMS) testing methodology and two IBM Faculty Partnership Awards. He is a Fellow of the IEEE, served as the 2011 Program Chair for the International Test Conference, and is the recipient of the 2006 Emerald Award for outstanding leadership in recruiting and mentoring minorities for advanced degrees in science and technology.