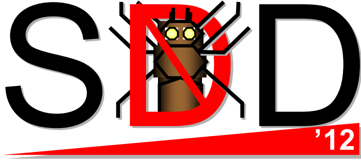

8th IEEE International Workshop on Silicon Debug and Diagnosis – SDD 2012

Thursday November 8th – Friday November 9th
Anaheim, California

Technical Program

Immediately following the 2012 International Test Conference

Thursday, November 8th

16:00 Opening Remarks
Brady Benware, Mentor Graphics, and **Nicola Nicolici**, McMaster University

16:15 Keynote Talk "*Post-Silicon Debug and Validation in the Billion Transistor SoC Era*"
Eric Rentschler, Fellow at AMD

17:00 Break and Poster Session (see next page for the list of posters)

17:30 Session 1 "*Bridging Pre- and Post-Silicon Validation*"
Moderator: **Eli Chiprout**, Intel Corp

"*Bridging Pre- and Post-Silicon Verification Through FPGA Prototyping and Embedded Instrumentation: Current Practices and Future Directions*"
Brad Quinton, Tektronix

17:50 Panel "*Coverage Metrics in Post-Silicon Validation*"
Rob Aitken, ARM
Darrell Carder, Freescale
Chuck Fleckenstein, Intel Corp
Dennis Wittig, IBM

19:00 Workshop Reception

Friday, November 9th

08:00 Invited Address "*Improving Design, Manufacturing and Even Test through Test-Data Mining*"
Shawn Blanton, Professor of ECE and Director of the Center for Silicon System Implementation at Carnegie Mellon University

08:40 Session 2 "*Defect Diagnosis and Yield Learning*"
Moderator: **Bharath Seshadri**, nVidia

Talk 1: "*Overlaying Silicon Results with Design Profiling to Discover Systematic Yield Detractors*"
Shobhit Malik, **Thomas Herrmann** and **Sriram Madhavan**, GlobalFoundries
Chris Schuermyer and **Geir Eide**, Mentor Graphics
Talk 2: "*Defect Localization Accuracy by Means of Effect-Cause Intra-Cell Diagnosis at Transistor Level*"
Zhenzhou Sun, Alberto Bosio, Luigi Dilillo, Patrick Girard, Aida Todri and **Arnaud Virazel,** LIRMM
Etienne Auvray, ST Microelectronics
Talk 3: "*Coarse Set-Based Defect Diagnosis*"
Jason Doege and **Joshua Torrey**, AMD
Talk 4: "*Systematic Open Via Diagnosis Based on Physical Features*"
Po-Juei Chen, Chieh-Chih Che and **James C.-M. Li**, National Taiwan University

10:00 Break and Poster Session (see next page for the list of posters)

10:30 Session 3 "*Digital and Analog Diagnosis and Validation*"
Moderator: **Davide Appello**, ST Microelectronics

Talk 1: "*Volume Diagnostics with Static Timing Analysis to Improve Yield on Transition Fault Test Patterns*"
Christophe Suzor and **Salvatore Talluto**, Synopsys
Nelly Feldman, ST Microelectronics
Talk 2: "*Capturing Variability in Pre-Silicon Delay Models for Post-Silicon Tasks: Pin-to-Pin and Beyond*"
Prasanjeet Das and **Sandeep Gupta**, University of Southern California
Talk 3: "*Using Dynamic Laser Stimulation (DLS) to Accelerate Scan Chain Debug and Defect Localization*"
Izak Kapilevich and **Cathy Kardach**, DCG Systems, Inc.
Talk 4: "*Signature Testing for Post Silicon Validation of RF/Analog Circuits*"
Abhijit Chatterjee, Sabyasachi Deyati, Barry Muldrey, Shyam Devarakond, Aritra Banerjee and **Michael Giardino**, Georgia Tech

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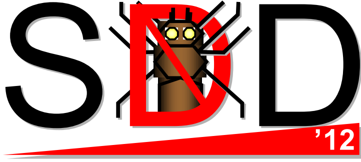

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Friday, November 9th (continued from the previous page)

12:00 Lunch

13:00 Session 4 "*Design-for-Debug and Case Studies*"
Moderator: **Sandeep Gupta**, University of Southern California

Talk 1: "*Evolution of Graphics NorthBridge Test and Debug Architectures Across Four Generations of AMD Fusion APUs*"
Arie Margulis, David Akselrod and **Mike Ricchetti**, AMD
Talk 2: "*Physical Design for Debug – A Low Cost Method to Extend DFT*"
John Giacobbe, Intel Corp
Talk 3: "*Recent Case-Studies of Debugging Power and Reset Related Failures*"
Nayana Prakash, Sanjay Krishna, Ranga Konduri, Abhijeet Shrivastava, Srinivas Vooka, Venkatraman Ramakrishnan and **Srivaths Ravi**
Texas Instruments

14:00 Break

14:30 Session 5 "*Infrastructure Support for Debug and Validation*"
Moderator: **Paolo Bernardi**, Politecnico di Torino

Talk 1: "*System Level Instrumentation Using the Nexus 5001-2012 Specification*"
Neal Stollon, The Nexus 5001 Forum and HDL Dynamics
Talk 2: "*Towards Simulator-like Visibility in FPGAs*"
Eddie Hung and **Steve Wilton**, University of British Columbia
Talk 3: "*Time to Market Reduction from Pre-/Post-Silicon Verification to Production on ATE*"
Atsuo Sawara and **Angarai Sivaram**, Advantest Corp
Talk 4: "*An iJTAG based Solution for Testing And Debug of Embedded IP*"
Givargis Danialy, Martin Keim and **Liyang Lai**, Mentor Graphics

15:50 Closing Remarks
Brady Benware, Mentor Graphics, and **Nicola Nicolici**, McMaster University

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Poster Session on Thursday, November 8th, at 17:00 and Friday, November 9th, at 10:00

Poster 1: "*Case Study of Silicon Debug and Design for Debug of a Complex System On Chip*"
Pranay Kotasthane, Bipin Duggal, Vivek Balram, Guruprasad Poonja and **Nagasuma Shashidhara,** Texas Instruments
Poster 2: "*Clean the Corners: Leveraging Pre-Silicon Verification Corner Cases to Post-Silicon Debug*"
Zelong Sun *and* **Qiang Xu,** The Chinese University of Hong Kong
Poster 3: "*Hierarchical Multi-Agent Approach for DFx Logic Verification in APUs*"
Jose-Antonio Cruz-Pastora, Francisco Duran-Urrea and **David Akselrod,** AMD
Poster 4: "*Mutation Based Debugging Technique with Auto-Correction Mechanism for RTL Designs*"
Payman Behnam, Bijan Alizadeh and **Zainalabedin Navabi,** University of Tehran, and **Masahiro Fujita,** University of Tokyo
Poster 5: "*A SBST Approach to Test Data Hazards Mechanisms in Pipelined Microprocessors*"
Paolo Bernardi, Ernesto Sanchez, Lyl Ciganda, Matteo Sonza Reorda and **Michelangelo Grosso,** Politecnico di Torino
Oscar Ballan, ST Microelectronics
Poster 6: "*Reduced-Complexity Trojan Detection Method via Delay Measurements*"
Jianwei Zhang, Byeongju Cha and **Sandeep Gupta**, University of Southern California
Poster 7: "*A Case Study on the Benefits of Functional Memory Access During ATE Test and Fault Isolation Techniques for Embedded SRAM*"
Corey Goodrich, Texas Instruments
Poster 8: "*Mutation Analysis with Coverage Discounting*"
Peter Lisherness, Nicole Lesperance and **Tim Cheng**, University of California, Santa Barbara